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imagination, and creativity. Digital design starts with RTL such as Verilog or VHDL, but it is only the beginning. A complete designer needs to have a good understanding of the Verilog language, digital design techniques, system architecture, IO protocols, and hardware-software interaction. Some

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of it will come from experience, and some will come with concerted effort. Graduating from college and entering into the world of digital system design becomes an overwhelming task, as not all the information is readily available. In this book, we have made an effort to explain the concepts in a

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simple way with real-world examples in Verilog. The book is intended for digital and system design engineers with emphasis on design and system architecture. The book is broadly divided into two sections - chapters 1 through 10, focusing on the digital design aspects and chapters 11

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through 20, focusing on the system aspects of chip design. This book can be used by students taking digital design and chip design courses in college and availing it as a guide in their professional careers. Chapter 3 focuses on the synthesizable Verilog constructs, with examples on reusable

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design (parameterized design, functions, and generate structure).

Chapter 5 describes the basic concepts in digital design - logic gates, truth table, De Morgan's theorem, set-up and hold time, edge detection, and number system. Chapter 6 goes into details of digital design explaining

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larger building blocks such as LFSR, scrambler/descramblers, error detection and correction, parity, CRC, Gray encoding/decoding, priority encoders, 8b/10b encoding, data converters, and synchronization techniques. Chapter 7 and 8 bring in advanced concepts in chip design and

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architecture - clocking and reset strategy, methods to increase throughput and reduce latency, flow-control mechanisms, pipeline operation, out-of-order execution, FIFO design, state machine design, arbitration, bus interfaces, linked list structure, and LRU usage and

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Implementation. Chapter 9 and 10 describe how to build and design ASIC/SoC. It talks about chip micro-architecture, partitioning, datapath, control logic design, and other aspects of chip design such as clock tree, reset tree, and EEPROM. It also covers good design practices, things to avoid

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and adopt, and best practices for high-speed design. The second part of the book is devoted to System architecture, design, and IO protocols. Chapter 11 talks about memory, memory hierarchy, cache, interrupt, types of DMA and DMA operation. There is Verilog RTL for a typical DMA

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controller design that explains the scatter-gather DMA concept.

Chapter 12 describes hard drive, solid-state drive, DDR operation, and other parts of a system such as BIOS, OS, drivers, and their interaction with hardware. Chapter 13 describes embedded systems and internal buses

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such as AHB, AXI used in embedded design. It describes the concept of transparent and non-transparent bridging. Chapter 14 and chapter 15 bring in practical aspects of chip development - testing, DFT, scan, ATPG, and detailed flow of the chip development cycle (Synthesis, Static

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timing, and ECO). Chapter 16 and chapter 17 are on power saving and power management protocols. Chapter 16 has a detailed description of various power savings techniques (frequency variation, clock gating, and power well isolation). Chapter 17 talks about Power Management protocols

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such as system S states, CPU C states, and device D states. Chapter 18 explains the architecture behind serial-bus technology, PCS, and PMA layer. It describes clocking architecture and advanced concepts such as elasticity FIFO, channel bonding (deskewing), link aggregation, and

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analysis. At each step, problems related to each phase of the design flow are identified, with solutions and work-arounds described in detail. In addition, crucial issues related to layout, which includes clock tree synthesis and back-end integration (links to layout) are also discussed at

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who is involved in the ASIC design methodology, starting from RTL synthesis to final tape-out. Target audiences for this book are practicing ASIC design engineers and graduate students undertaking advanced courses in ASIC chip design and DFT techniques. From the Foreword: `This

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practicing ASIC design engineers as well as to students of advanced VLSI courses in ASIC design'. Dr Dwight W. Decker, Chairman and CEO, Conexant Systems, Inc., (Formerly, Rockwell Semiconductor Systems), Newport Beach, CA, USA.

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