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Electromigration (EM) is a major reliability problem for on-chip interconnects. With the trend of shrinking wire dimensions and higher current densities, EM concerns emerge. In this thesis, we mainly investigate EM problems in power grids. We provide design guidelines and CAD solutions to improve full-chip EM reliability for power grids. Current density is the most important factor that affects interconnect EM lifetime. We demonstrate that the widely held belief that the worst grid currents occur when all current sources are turned on is misleading. We study the correlation between current sources and wire currents, and use linear programming to determine true worst case currents on power grid wires. Temperature is another important factor since EM lifetime has an exponential dependency on temperature. In modern designs, wire Joule heating causes a non-negligible temperature rise above substrate, which is not taken into account in many EM reliability check tools. We propose a two stage thermal analysis to efficiently estimate wire temperatures for EM analysis purpose. Today, process variations affect circuit behavior significantly, including EM. We study the effect of chemical mechanical planarization (CMP) dishing and lithography edge placement error (EPE) on EM. Variation tolerance of each wire is determined as a design aid. In power grids, via arrays are widely used for inter-layer connections, their EM behavior is very different from that of a single via. We develop a compact model to quickly determine current distribution in a via array, and numerically obtain via array EM lifetime using Monte-Carlo method. We notice that a power grid provides plenty of redundancy such that not all via arrays are crucial to power integrity. This inherent redundancy allows us to explore the trade-off between EM reliability and power grid integrity. We develop a heuristic power track upsizing algorithm to minimize the extra metal used for EM reliability budget.