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The recent boom in the mobile telecommunication market has trapped the interest of almost all electronic and communication companies worldwide. New applications arise every day, more and more countries are covered by digital cellular systems and the competition between the several providers has caused prices to drop rapidly. The creation of this essentially new market would not have been possible without the ap pearance of smalI, low-power, high-performant and certainly low-cost mobile termi nals. The evolution in microelectronics has played a dominant role in this by creating digital signal processing (DSP) chips with more and more computing power and com bining the discrete components of the RF front-end on a few ICs. This work is situated in this last area, i. e. the study of the full integration of the RF transceiver on a single die. Furthermore, in order to be compatible with the digital processing technology, a standard CMOS process without tuning, trimming or post-processing steps must be used. This should flatten the road towards the ultimate goal: the single chip mobile phone. The local oscillator (LO) frequency synthesizer poses some major problems for integration and is the subject of this work. The first, and also the largest, part of this text discusses the design of the Voltage Controlled Oscillator (VCO). The general phase noise theory of LC-oscillators is pre sented, and the concept of effective resistance and capacitance is introduced to char acterize and compare the performance of different LC-tanks.

Interest in latchup is being renewed with the evolution of complimentary metal-oxide semiconductor (CMOS) technology, metal-oxide-semiconductor field-effect transistor (MOSFET) scaling, and high-level system-on-chip (SOC) integration. Clear methodologies that grant protection from latchup, with insight into the physics, technology and circuit issues involved, are in increasing demand. This book describes CMOS and BiCMOS semiconductor technology and their sensitivity to present day latchup phenomena, from basic over-voltage and over-current conditions, single event latchup (SEL) and cable discharge events (CDE), to latchup domino phenomena. It contains chapters focusing on bipolar physics, latchup theory, latchup and guard ring characterization structures, characterization testing, product level test systems, product level testing and experimental results. Discussions on state-of-the-art semiconductor processes, design layout, and circuit level and system level latchup solutions are also included, as well as: latchup semiconductor process solutions for both CMOS to BiCMOS, such as shallow trench, deep trench, retrograde wells, connecting implants, sub-collectors, heavily-doped buried layers, and buried grids – from single- to triple-well CMOS; practical latchup design methods, automated and bench-level latchup testing methods and techniques, latchup theory of logarithm resistance space, generalized alpha (a) space, beta (b) space, new latchup design methods – connecting the theoretical to the practical analysis, and; examples of latchup computer aided design (CAD) methodologies, from design rule checking (DRC) and logical-to-physical design, to new latchup CAD methodologies that address latchup for internal and external latchup on a local as well as global design level. Latchup acts as a companion text to the author ' s series of books on ESD (electrostatic discharge) protection, serving as an invaluable reference for the professional semiconductor chip and system-level ESD engineer. Semiconductor device, process and circuit designers, and quality, reliability and failure analysis engineers will find it informative on the issues that confront modern CMOS technology. Practitioners in the automotive and aerospace industries will also find it useful. In addition, its academic treatment will appeal to both senior and graduate students with interests in semiconductor process, device physics, computer aided design and design integration.

The purpose of this book is to provide a complete working knowledge of the Complementary Metal-Oxide Semiconductor (CMOS) analog and mixed-signal circuit design, which can be applied for System on Chip (SOC) or Application-Specific Standard Product (ASSP) development. It begins with an introduction to the CMOS analog and mixed-signal circuit design with further coverage of basic devices, such as the Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) with both long- and short-channel operations, photo devices, fitting ratio, etc. Seven chapters focus on the CMOS analog and mixed-signal circuit design of amplifiers, low power amplifiers, voltage regulator-reference, data converters, dynamic analog circuits, color and image sensors, and peripheral (oscillators and Input/Output [I/O]) circuits, and Integrated Circuit (IC) layout and packaging. Features: Provides practical knowledge of CMOS analog and mixed-signal circuit design Includes recent research in CMOS color and image sensor technology Discusses sub-blocks of typical analog and mixed-signal IC products Illustrates several design examples of analog circuits together with layout Describes integrating based CMOS color circuit

"Symbolic analyzers have the potential to offer knowledge to sophomores as well as practitioners of analog circuit design. Actually, they are an essential complement to numerical simulators, since they provide insight into circuit behavior which numerical "